REMARKS

Claims 1-5, 7-12, 14-25, and 27, all the claims pending in the application, stand rejected on prior art grounds. Claims 1, 8, and 21 stand rejected upon informalities. Applicants respectfully traverse these rejections based on the following discussion.

I. Request For Withdrawal Of Final Rejection

The Applicants respectfully request that the Examiner withdrawal the final rejection as the final rejection failed to comply with the requirements of 37 C.F.R. §1.113 and MPEP §706.07, wherein in making a final rejection the Examiner must state all grounds of rejection then considered applicable to the claims in the application, clearly stating the reasons in support thereof. Specifically, the Applicant's submit the Examiner did not consider the claim amendments in the response filed in accordance with 35 U.S.C. §1.111 on 3/1/07. Rather the Examiner continued to reject the claims as presented prior to 3/1/07 and did not consider the additional features amended into the claims.

For example, in rejecting claims 1 and 21, pages 6-7 of the final office action in refer to the previously claimed features in claim 1 (and the similar features in claim 21) of "perform a regression analysis on historical costs of historical critical gate dimensions at said fabricator, using said historical critical gate dimensions as independent variables and said historical costs as dependent variables"; "create, in said database, models from said regression analysis only showing a relationship between said historical critical gate dimensions and said historical costs"; and "predict product costs of said new device based on said models". However, per the response filed on 3/1/07 these features in claim 1 were amended to read "perform a regression analysis

using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs" and "predict product costs of said new device based on said user inputs and said relationship curves." No where in the final office action does the Examiner address features amended into claims 1 and 21, much less clearly state all grounds for rejecting claims 1 and 2, as amended. Similarly, in rejecting independent claim 8, pages 7-8 of the final office action do not address the features amended into independent claim 8 per the 3/1/07 response.

In view of the foregoing, the Examiner is respectfully requested to withdraw the final rejection and issue another office action in which each of the claim features are considered such that all grounds supporting the rejection of the claims, as currently presented, are stated.

II. The 35 U.S.C. §112, First Paragraph, Rejection

Claims 1, 8, and 21 stand rejected under 35 U.S.C. §112, first paragraph. These rejections are traversed as explained below. The Examiner has indicated that claims 1, 8 and 21 contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the Examiner was unable to locate the following feature "wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs." The Applicants respectfully disagree.

As disclosed in the specification at paragraph [0008], the invention performs "a regression analysis on historical costs of historical critical dimensions at a fabrication, using the historical critical dimensions as independent variable and the historical costs as dependent variables. Then models are created from this regression analysis so that costs of a new device can be predicted. More specifically, paragraphs [0017]- [0021], disclose that the invention is able to predict the costs of unknown technology generations by looking "at historical costs for technologies producing different gate dimensions to predict the cost of further technologies that produce even smaller gate dimensions." The invention performs a regression analysis on all technologies currently running in a fabricator. This regression analysis is performed by treating the lithography generation (or critical gate dimension) as the independent variable and the wafer cost as the dependent variable to produce relationship curves (as illustrated in FIG. 1). The curves of Figure 1 represents a "relationship between cost and technology generation (critical gate dimension lithographic groundrules)." Paragraph [0021] indicates that Figure 1 is an example of relationships between technology critical dimension and costs for a particular semiconductor fabricator and can be used by that semiconductor fabricator to project costs of further unknown technologies. Paragraph [0038] further clarifies that a regression analyzer performs the regression analysis (i.e., performs a least-square analysis) on the historical data 40 (i.e., data contained in the database the historical costs and historical critical gate dimensions) from the different technologies to create the critical dimensions/cost relationships (i.e., the relationship curves of FIG. 1). In view of the foregoing, the specification clearly indicates that the regression analysis produces relationship curves that show relationships between historical

critical gate dimensions and historical costs and further does not indicate that the regression analysis produces relationship curves that show any other relationships.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. The 35 U.S.C. §112, Second Paragraph, Rejection

Claim 1 stands rejected under 35 U.S.C. §112, second paragraph. This rejection is traversed as explained below. The Examiner is unable to determine what the applicant is claiming by the claim 1 language of "perform a regression" and further that there is insufficient antecedent basis for "said regression analysis". Obviously, the word "analysis" was inadvertently deleted from line 9 in the previous amendment. Claim 1 is amended herein to overcome the rejection by adding the word "analysis" back into the claims such that line 9 reads "perform a regression analysis" and this feature is the antecedent basis for "said regression analysis". In view of the foregoing, the Examiner is respectfully requested to enter the amendment (as no new issue is raised which would require a new search) and to reconsider and withdraw this rejection.

IV. The Prior Art Rejections

Claims 1-5, 7-12, 14-25, and 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over "21st Century Semiconductor Manufacturing Capabilites," hereinafter referred to as Manufacturing, in view of Evans, et al. (U.S. Patent No. 6,775,647), hereinafter referred to as Evans. Applicants respectfully traverse these rejections because the final office action fails to

establish a prima facie case of obviousness under MPEP§2141-2143. Specifically, the prior art references cited refer to non-analagous prior art. Additionally, there is no suggestion or motivation to combine the referenced teachings, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Finally, even if the cited references were to be considered analogous art and even if a motivation to combine were present, the references fail to teach or suggest all of the claim limitations.

A. Summary Of The Present Invention.

The present invention was designed to provide an economic and efficient method and system that can predict the cost per wafer for future generations of technologies based solely upon historical data of known technologies. Per paragraph [0017]-0019], the invention accomplishes this by extrapolating current costs of different technologies to future technologies. More specifically, in silicon-based technology, the generations are defined by relatively large reductions in the dimensions of the gate conductor in a transistor structure. The invention performs regression analysis on historical costs for all technologies currently running in a fabricator by treating the lithography generation (or critical gate dimension) as the independent variable and wafer cost as the dependent variable. The regression analysis produces a relationship curve (see FIG. 1) between cost and technology generation (i.e., between cost and critical gate dimension lithographic groundrule). Cost models are created based on the relationship curves. Then, to predict cost of a future technology, a calculator or computer can be utilized as the cost prediction unit which takes user input regarding a new technology (e.g., new design parameters and new critical dimension for a new device) through a user interface and

calculates the cost prediction for the new technology based upon the critical dimensions/cost relationship (see paragraphs [0008-0009]and [0038]).

B. Summary Of Cited Prior Art References

1. Manufacturing.

Manufacturing is a paper that broadly discusses responses of semiconductor industry management and university faculty to the predictions of Moore's Second Law, which states that one of the challenges of Moore's First Law (i.e., semiconductor device complexity doubles every 18 months) is that facility costs increase on a semi-log scale (see Abstract). It does not disclose any specific method or system, much less a method or system for predicting semiconductor product costs at a fabricator.

Figures 1-3 and Tables 1-3 of Manufacturing illustrate industry-wide data related to following Moore's First Law. Specifically, Figure 1 illustrates Moore's First Law (i.e., that chip complexity defined by the number of active elements on a single chip increases (see y-axis) with time (see x-axis)). Figure 2 breaks it down into cost per function (i.e., cost per chip element) over time and illustrates that while the cost per function continues to decrease the rate at which it decreases has slowed. Table 1 illustrates programs associated with Moore's First Law and their consequences (e.g., consequences related to feature size reduction, chip size increases, wafer diameter, yield, etc.). Figure 3 further illustrates cost trends related to following Moore's First Law (i.e., Figure 3 illustrates Moore's Second Law). That is, Figure 3 is a graph illustrating that the costs per factory (right side of graph) increase in conjunction with the increase in chip complexity (defined as the number of active elements on a chip on the left side of the graph) over time (x-axis). Table 2 is the same as Table 1 but further illustrates the addition of equipment

cost and operational efficiency associated with Moore's First Law. In light of this information, Manufacturing recognizes two problems with regard to cost per chip element and factory cost containment: (1) programs that lower cost per element can add to factory cost; and (2) some programs have diminishing returns. Manufacturing further discusses generally semiconductor industry responses to these problems, including, for example, operational modeling and simulations (OM&S) to lower manufacturing costs and speed up the process of trying alternative solutions to different operational scenarios (see page 4, col. 1).

2. Evans.

Per the Summary section, Evans discloses a method and system for estimating process-oriented manufacturing costs of a product (e.g., an aircraft engines) based on the costs associated with different part designs (e.g., engine part designs). The method and system performs a regression analysis on the various part designs and configurations and generates cost models for those part designs and configurations. Using the cost models, both the manufacturing costs associated with individual part designs and the product costs as a whole can be estimated.

More specifically, Evans discloses the use of a regression analysis to establish a relationship between the features of a specific part and multiple different processing costs related to achieving those features (see step 35 of Figure 2). The cited portion of Evans (column 5, lines 18-50) describes developing a cost model for a family of parts in an aircraft engine (e.g., a guide vane/diffuser family). The model is defined by the alternate designs for the part and the different configurations and material applications for each design. Then, manufacturing costs for each of the different configuration of each of the different design variations in each of the different material selections are estimated based on the processes used to manufacture the part (see col. 5,

line 65-col. 6, line 2). Next a cost model for the entire family of parts is built using a regression analysis (col. 7, line 19). Then, resource data, including the cost model algorithms for each family of parts, are gathered for the designing and cost estimation of a complete engine. This invention allows a user to select specific part designs and configurations for each sub-component that is to be incorporated into the engine in order to estimate the manufacturing costs associated with the part itself and/or the manufacturing cost associated with the engine as a whole (see col. 7, line 61-col. 8, line 65 and col. 9, lines 26-43; Abstract).

C. Non-Analagous Art

The Applicants submit that neither Manufacturing, nor Evans represent art analogous to the present invention as required by MPEP §2141. Specifically, it is well known that "In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicants endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." (See *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992).

The Applicants submit that Manufacturing is not an analogous prior art reference because Manufacturing does not discuss a system and method for predicting semiconductor product costs (i.e., the product costs of a new device) at a fabricator. Rather, per the Abstract, Manufacturing deals with responses of semiconductor industry management to the Moore's Laws (i.e., semiconductor device complexity doubles every 18 months and facility costs increase on a semi-log scale with increases in device complexity). The industry responses include logistics control, inventory management, better facility design, supplier management programs, etc. Special attention is paid in to knowledge management and operational modeling and simulation

technology (OM&S), which are used to affect factory performance. No where in Manufacturing does it disclose that any of the techniques are used to predict the actual product costs for a new technology. Consequently, the Applicants disagree with the Examiner's assertion that Manufacturing relates to the same field of endeavor of "predicting semiconductor product costs at a fabricator" as the present invention or that Manufacturing discloses information that is reasonably pertinent to the particular problem with which the inventor was concerned.

The Applicants further submit that Evans is not an analogous prior art reference. The final office action notes that Manufacturing does not expressly disclose performing a regression analysis on historical costs of historical critical gate dimensions. To cure this deficiency, the office action refers to Evans for teaching a method of estimating manufacturing costs using a regression analysis. However, due to the unique nature of the semiconductor manufacturing industry, the estimation of the manufacturing costs associated with products, such as the aircraft engines of Evans, are not "reasonably pertinent to the particular problem with which the inventor is concerned". More specifically, as mentioned above and stated in the Abstract of Manufacturing, the semiconductor industry generally adheres to Moore's Laws (i.e., device complexity doubles about every 18 months and facility costs increase on a semi-log scale). Other manufacturing industries, such as aircraft manufacturing industries, do not adhere to these laws. Thus, methods of cost predictions in other manufacturing industries would not be reasonably pertinent to cost predictions methods in the semiconductor manufacturing industries.

Furthermore, it would not be reasonable for an individual interested in predicting costs for a new semiconductor design to look to different manufacturing industries because of the unique nature of the cost impact of specific components of semiconductor products.

Specifically, those skilled in the art will recognize that the semiconductor product component dimensions (e.g., gate dimensions, source and drain dimensions, channel dimensions, gate oxide dimensions, spacer dimensions, etc.) tend to decrease with each new technology generation. However, the impact of one feature alone, namely gate dimension, is unique to the semiconductor manufacturing industry. That is, semiconductor product costs increase exponentially with the decreasing gate dimension. Thus, the semiconductor manufacturing industry would not benefit from the teachings found within non-semiconductor manufacturing industries, such as the aircraft engine manufacturing, where size scaling is not the trend and where costs are not known to increase exponentially with the decreasing dimension of a particular component of the product being manufactured. Therefore, the Applicants submit that a reference to an aircraft manufacturing industry cost prediction method should not be considered reasonably pertinent to the particular problem with which the inventor was concerned (i.e., cost predictions for a semiconductor product at a fabricator based on gate dimension).

D. Lack of Motivation to Combine Manufacturing and Evans.

The Examiner further asserts that the "motivation is in the reference (see Evans; col. 3, lines 7-34 and col. 5, lines 19-39) and is reasonably pertinent to the particular problem with which the applicant is concerned." More specifically, the final office action provides on page 6 that "Since Evans et al. and Manufacturing are both from the same field of endeavor of predicting a cost for developing new products, the purpose disclosed by Evans et al. would have been well recognized in the pertinent field of Manufacturing. Therefore, it would have been obvious at the time of the invention was made to a person having ordinary skill in the ad to modify the invention of Manufacturing such that the invention performs a regression analysis

based on a relationship between the historical gate dimensions and the costs (see Fig. 2 and Table 1 of Manufacturing), as taught by Evans et al. for the purpose of providing an advantage of cost modeling for an engineer who is striving for a better understanding of the cost of his design and seeking to reduce production costs."

The Applicants respectfully disagree because, as discussed above, Manufacturing refers to trends in the semiconductor manufacturing industry for improving facility performance in response to Moore's Laws, which are unique to the semiconductor manufacturing industry. It does not disclose estimating actual product costs of a new device at a fabricator. Contrarily, Evan relates to estimating the costs of part design variations as well as their impact on overall product costs (e.g., the costs associated with a particular guide van design as well as its impact on the overall aircraft engine manufacturing costs). Since the problems addressed in Manufacturing are size-scaling and Moore's Laws and since the disclosed responses to those problems relate to improving facility performance and not to predicting product costs of a new device, there would be no reason or motivation to combine the teachings of Manufacturing with the Evans method of predicting part design manufacturing costs. The lack of motivation to combine is further supported by the fact that Manufacturing and Evans relate to completely different industries (i.e., the semiconductor manufacturing industry and the aircraft manufacturing industry, respectively) and that only in the semiconductor manufacturing industry are size-scaling and Moore's Law a significant concern (i.e., size-scaling and Moore's Laws are unique to the semiconductor manufacturing industry).

3. Failure Of Manufacturing And Evans In Combination To Disclose Several Of The Patentable Features Of Independent Claims 1, 8, 15 and 21.

The proposed combination of Manufacturing and Evans fails to teach or suggest the following features of independent claim 1 or the similar features found in independent claims 8, 15 and 21: (1) "a storage medium including a database of historical costs and historical critical gate dimensions of different technologies run at said fabricator"; (2) "a user interface adapted to receive user inputs for new design parameters and new critical gate dimensions associated with a new device to be produced at said fabricator"; (3) "perform a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs"; and (4) "predict product costs of said new device based on said user inputs and said relationship curves".

More particularly, the final office action cites Manufacturing as disclosing: (1) a system and method for predicting semiconductor product costs at a fabricator; (2) "a storage medium including a database of historical critical gate dimensions and historical critical ground rules correlated to cost functions at said fabricator (page 1, FIGS. 2-3: Tables 1-3)"; (3) "a user interface (keyboard or mouse) having user inputs for new design parameters and new critical gate dimensions associated with a new device to be produced at said fabricator"; (4) "receive said user inputs (see especially Figs. 2-3, Tables 1-3 and Supra Response to Applicant's Argument)"; (5) "create, in said database, models from said regression analysis only showing a relationship between said historical critical gate dimensions and said historical costs (see Supra Figs. And Tables)"; and (6) "input new design parameters and new critical gate dimensions of a new device into the database and predicting product costs of the new device based on the models (see the entirety of the document, to note how "Operational modeling and simulation" and

"Knowledge Management" work to compute the costs for the new design)." The Examiner further acknowledges that Manufacturing fails to disclose a regression analysis on historical costs of historical critical gate dimensions at a specific fabricator and then uses the historical critical gate dimensions as independent variables and the historical costs as dependent variables in order to produce models as recited in the claims. Thus, the Examiner cites col. 5, lines 19-38 of Evans as teaching an invention that performs a regression analysis for developing new products. The Applicants respectfully disagree.

As discussed above, Manufacturing is a paper that discusses "responses of industry management and university faculty to the predictions of Moore's Second Law". Moore's Second Law states that one of the challenges of Moore's First Law (i.e., device complexity doubles every 18 months) is that facility costs increase on a semi-log scale (see Abstract). Figures 1-3 and Tables 1-3 of Manufacturing illustrate data related to Moore's First and Second Laws within the entire semiconductor industry. That is, Figure 1 illustrates Moore's First Law (i.e., that chip complexity defined by the number of active elements on a single chip increases (see y-axis) with time (see x-axis)). Figure 2 breaks it down into cost per function (i.e., per chip element) over time. Table 1 illustrates that programs associated with Moore's First Law have consequences (e.g., consequences related to feature size reduction, chip size increases, wafer diameter, yield, etc.). Figure 3 further illustrates cost trends related to Moore's First Law (i.e., illustrates Moore's Second Law). That is, Figure 3 is a graph illustrating that the costs per factory (right side of graph) increase in conjunction with the increase in chip complexity (defined as the number of active elements on a chip on the left side of the graph) over time (x-axis). Table 2 is the same as Table 1 but further illustrates the addition of equipment cost and operational

efficiency associated with Moore's First Law. In light of this information Manufacturing recognizes two problems with regard to cost per chip element and factory cost containment: (1) programs that lower cost per element can add to factory cost; and (2) some programs have diminishing returns. Thus, rather than teaching a system and method for predicting semiconductor product costs at a fabricator, Manufacturing discusses semiconductor industry responses to these problems including, for example, operational modeling and simulations (OM&S) for improving facility performance.

No where in Manufacturing does it teach or disclose "a storage medium including a database of historical costs and historical critical gate dimensions of different technologies run at said fabricator." The cited portions of Manufacturing (i.e., page 1, FIGS. 2-3: Tables 1-3) refer to relative chip complexity (defined by the number of active elements on a single chip), average feature size reduction, average chip size reduction, average wafer diameter, relative operational efficiency, relative equipment cost, etc., from year to year (e.g., resulting from factory cost control programs (see table 2)) with predictions for future year(s). Thus, while the cited portions do disclose that historical data is maintained, they do not disclose a storage medium that specifically includes "a database of historical costs and historical critical gate dimensions of different technologies run at a fabricator."

No where in Manufacturing does it teach or disclose "a user interface adapted to receive user inputs for new design parameters and new critical gate dimensions associated with a new device to be produced at said fabricator" or "a computer adapted to receive said user inputs". Again, the cited figures and tables refer to relative chip complexity (defined by the number of active elements on a single chip), average feature size reduction, average chip

size reduction, average wafer diameter, relative operational efficiency, relative equipment cost, etc., from year to year with a prediction for future year(s). They do not disclose a system/method that allows a user to specifically input a new design and new critical gate dimensions associated with the new device to be produced at the fabricator.

No where in Manufacturing or a combination of Manufacturing and Evans does it teach or disclose a "a computer adapted to perform a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs." As mentioned above, the final office action provides that Manufacturing teaches a previously claimed feature of "create, in said database, models from said regression analysis only shown a relationship between said historical critical gate dimensions and said historical costs (see Supra Figs. And Tables)." However, the Examiner also acknowledges that Manufacturing fails to disclose "performing a regression analysis on historical costs of historical critical gate dimensions at said fabricator, using said historical critical gate dimensions as independent variables and said historical costs as dependent variables." Thus, the Examiner cites col. 5, lines 19-38 of Evans as teaching this feature. The Applicants respectfully disagree.

Again, the cited figures and tables of Manufacturing refer to relative chip complexity (defined by the number of active elements on a single chip), average feature size reduction, average chip size reduction, average wafer diameter, relative operational efficiency, equipment costs, etc., from year to year with a prediction for future year(s). They do not disclose actual

historical feature sizes, much less actual gate dimensions and a relationship between these actual historical gate dimensions and the costs of the product itself.

Furthermore, Evans discloses a method and system for estimating the manufacturing cost of an aircraft part design using regression analysis and basing an overall engine cost prediction based on the results of the regression analysis for all of the parts. However, Evans does not disclose using historical cost data to perform the regression analysis. More specifically, as discussed above, Evans requires that the dimensions of each part of an engine be specified in a regression analysis (see column 2, lines 19-34 and column 5, lines 19-39 of Evans). The regression analysis establishes a relationship between specific part features and multiple different processing costs related to achieving those features (see step 35 of Figure 2). That is, the cited portions of Evans (column 5, lines 18-50) describe developing a cost model for a family of parts in an aircraft engine (e.g., a guide vane/diffuser family). Specifically, using a regression analysis, the manufacturing costs (i.e., a cost model) for each of the configurations/designs is estimated based on the processes used to manufacture the part. The cost model is based on a set of discrete point estimates, not on historical cost data. That is, according to Evans (see col. 4 lines 34-44), "little or no historical cost data is available for the part using advanced materials and/or processes, [therefore] the cost model is derived from a set of discrete point estimates." Then, resource data, including the cost model algorithms for each family of parts, are gathered for the designing and cost estimation of a complete engine. That is, the user can select specific part designs and configurations for each sub-component that is to be incorporated into the engine in order to then estimate the total cost of the engine as a whole (see col. 7, line 61-col. 8, line 65; Abstract).

Because Evans is rooted in the technology of manufacturing aircraft engines, it does not address the unique aspects related to semiconductor manufacturing (e.g., the relationship between historical critical gate dimensions and historical costs), nor would it be expected to. In the semiconductor products, standard elements include, for example, source and drain regions, gates, gate oxides, channels, etc. The claimed invention is, however, able to predict the product costs of a new semiconductor device simply by specifying a new gate dimension, without having to specify dimensions, sizes, locations, thicknesses, etc. of any of these other elements. Equating the claimed ability to the aircraft engine manufacturing industry, would be like predicting the cost of an airplane engine based, for example, on the diameter of a single part of the engine. Evans clearly does not provide such teaching. Contrarily, if Evans' teaching were translated into the semiconductor manufacturing industry, Evans' cost models would be developed for all components of a semiconductor product (e.g., for gates, gate oxides, sources, drains, channels, contacts, etc.) and each cost model would be derived from a set of discrete points representing design variations and not derived from historical data. Consequently, the Applicants submit that no where in Manufacturing or a combination of Manufacturing and Evans does it teach or disclose a "a computer adapted to perform a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs."

No where in Manufacturing does it disclose "a computer adapted to predict product costs of said new device based on said user inputs and said relationship curves". The Examiner yet again indicates that this feature is disclosed in "the entirety of the document, to

note how "Operational modeling and simulation" and "Knowledge Management" work to compute the costs for the new design). 37 C.F.R. §1.104(c)(2) provides that "In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified." Given the nature of the Manufacturing paper, the Applicant's again submit that the citation of the Examiner does not sufficiently designate the particular part of Manufacturing relied upon by the Examiner to teach this feature.

Furthermore, the "Application of OM&S Technology" section of the Manufacturing paper does not disclose the claimed features of "inputting new design parameters and new critical gate dimensions of a new device into said database; and predicting product costs of said new device based on said relationship curves." As discussed above, Manufacturing addresses operational modeling and simulations (OM&S) generally indicating its purpose to lower manufacturing costs and speed up the process of trying alternative solutions to different operational scenarios (see page 4, col. 1). More specifically, page 4, col. 2 of Manufacturing indicates that "OM&S capabilities are directly linked to improvement of major factory performance metrics: cost reduction, delivery improvement, quality improvement or product performance improvement." No where in Manufacturing does it disclose that OM&S capabilities are linked to cost predictions, much less to cost predictions for a new device based on relationship curves that only show relationships between said historical critical gate dimensions and said historical costs.

In view of the foregoing, the Applicants submit that neither Manufacturing, nor Evans, teach or suggest the following features of features of independent claim 1 or the similar features found in independent claims 8, 15 and 21: (1) "a storage medium including a database of historical costs and historical critical gate dimensions of different technologies run at said fabricator"; (2) "a user interface adapted to receive user inputs for new design parameters and new critical gate dimensions associated with a new device to be produced at said fabricator"; (3) "perform a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs"; and (4) "predict product costs of said new device based on said user inputs and said relationship curves".

Therefore, independent claims 1, 8, 15 and 21 are patentable over "Manufacturing" in view of Evans. Further, dependent claims 2-5, 7, 9-12, 14, 16-20, 22-25 and 27 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

.

III. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, Applicants submit that claims 1-5, 7-12, 14-25, and 27, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. Therefore, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims and to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: July 10, 2007

/Pamela M. Riley/
Pamela M. Riley
Registration No. 40,146

Gibb & Rahman, LLC
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (410) 573-0227
Fax: (301) 261-8825
Customer Number: 29154